

Am79R79

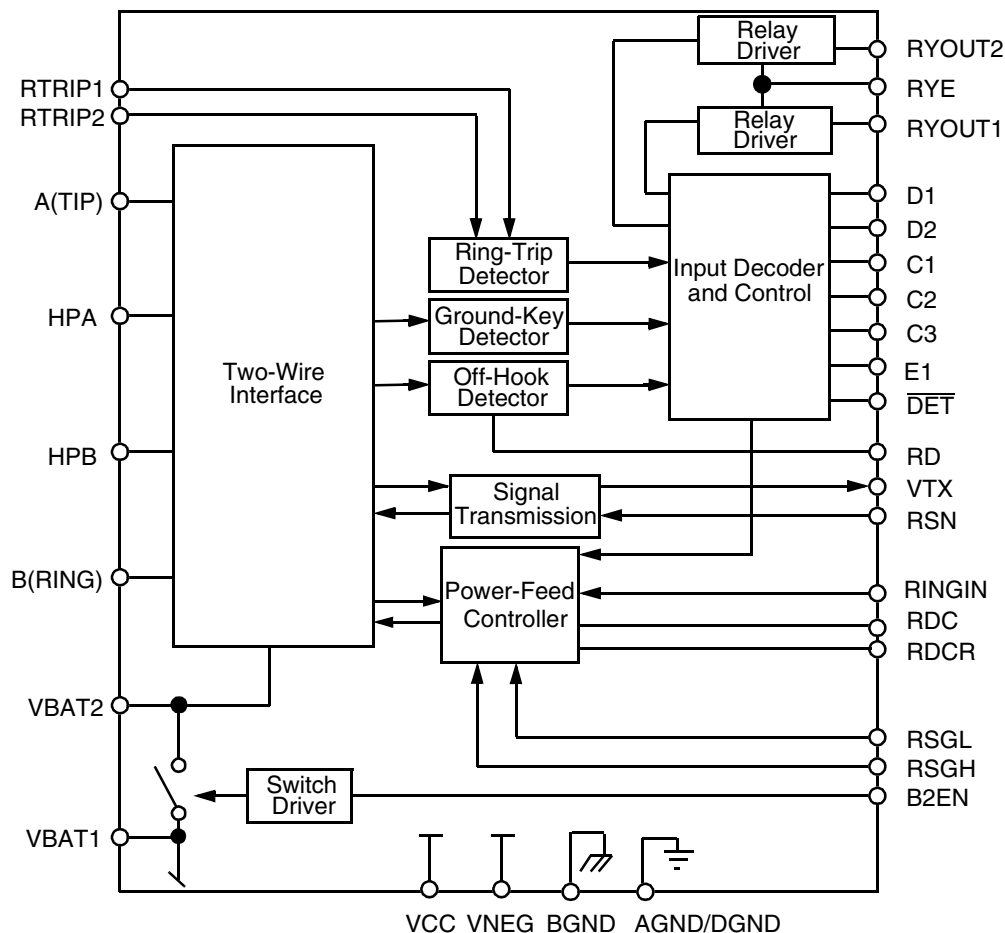
Ringing Subscriber Line Interface Circuit



DISTINCTIVE CHARACTERISTICS

- Ideal for short-loop applications
- Ideal for ISDN terminal adaptor and fixed radio access applications
- On-chip ringing with on-chip ring-trip detector
- Low standby state power
- Battery operation:
 - V_{BAT1} : -40.5 V to -75 V
 - V_{BAT2} : -19 V to V_{BAT1}
- On-chip battery switching and feed selection
- On-hook transmission
- Two-wire impedance set by single external impedance
- Programmable constant-current feed
- Programmable Open Circuit voltage
- Programmable loop-detect threshold
- Current gain = 1000
- Ground-key detector
- Tip Open state for ground-start lines
- Polarity reversal option available
- Internal V_{EE} regulator (no external -5 V power supply required)
- Two on-chip relay drivers and snubber circuits (32 PLCC)

BLOCK DIAGRAM



GENERAL DESCRIPTION

The Legerity family of subscriber line interface circuit (SLIC) products provide the telephone interface functions required throughout the worldwide market. Legerity SLIC devices address all major telephony markets including central office (CO), private branch exchange (PBX), digital loop carrier (DLC), fiber-in-the-loop (FITL), radio-in-the-loop (RITL), hybrid fiber coax (HFC), and video telephony applications.

The Legerity SLIC devices offer support of BORSHT (battery feed, overvoltage protection, ringing, supervision, hybrid, and test) functions with features including current limiting, on-hook transmission, polarity reversal, Tip Open, and loop-current detection. These features allow reduction of linecard cost by minimizing component count, conserving board space, and supporting automated manufacturing.

The Legerity SLIC devices provide the two- to four-wire hybrid function, DC-loop feed, and two-wire supervision. Two-wire termination is programmed by a scaled impedance network. Transhybrid balance can be achieved with an external balance circuit or simply programmed using a companion Legerity codec device, the Am79C02/03/031 DSLAC™ device, the Am79Q02/021/03 Programmable Quad SLAC (QSLAC™) device, or the Am79Q5457/4457 Nonprogrammable QSLAC device.

The Am79R79 Ringing SLIC device is a bipolar monolithic SLIC that offers on-chip ringing. Now designers can achieve significant cost reductions at the system level for short-loop applications by integrating the ringing function on chip. Examples of such applications

would be ISDN terminal adaptors, fiber-in-the-loop, radio-in-the-loop, hybrid fiber/coax and video telephony (home-side) boxes. The Am79R79 Ringing SLIC can provide sufficient voltage to meet the stringent LSSGR five-ringer equivalent specification. Using a CMOS-compatible input waveform and wave shaping R-C network, the Am79R79 Ringing SLIC can provide trapezoidal wave ringing to meet various design requirements.

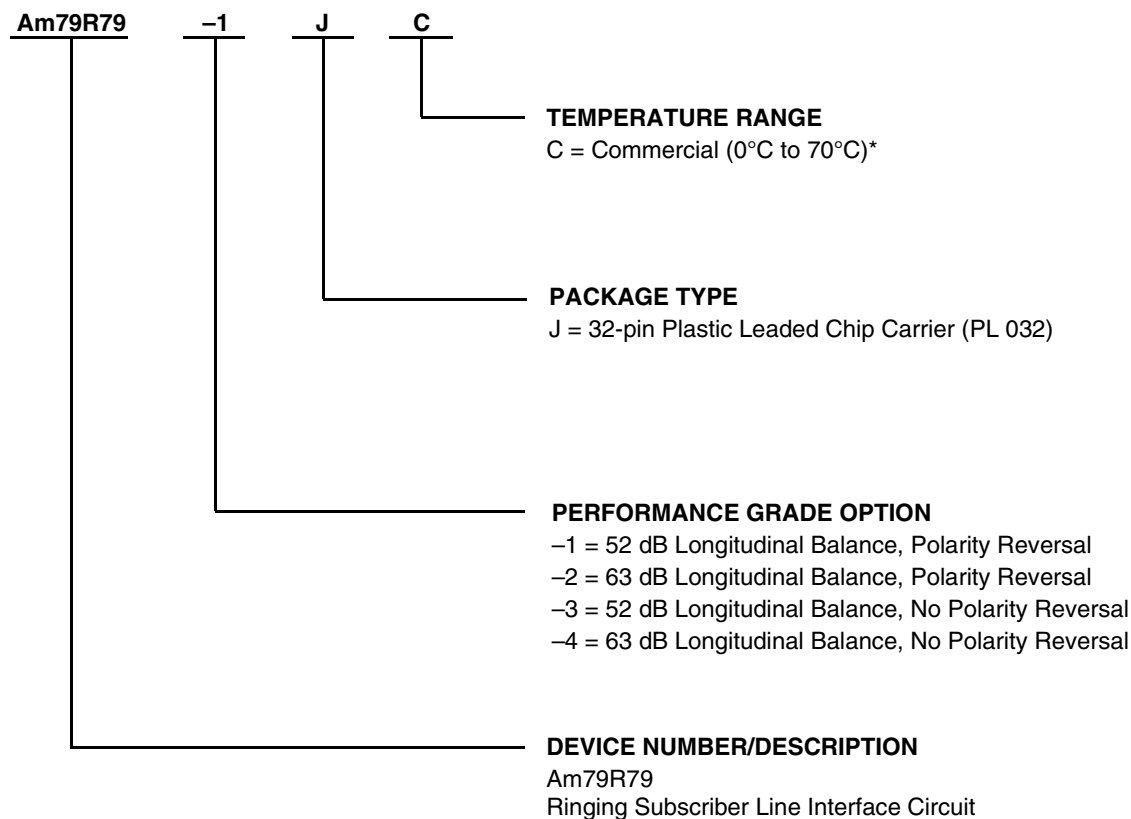
In order to further enhance the suitability of this device in short-loop, distributed switching applications, Legerity has maximized power savings by incorporating battery switching on chip. The Am79R79 Ringing SLIC device switches between two battery supplies such that in the off-hook (active) state, a low battery is used to save power. In order to meet the Open Circuit voltage requirements of fax machines and maintenance termination units (MTU), the SLIC automatically switches to a higher voltage in the on-hook (standby) state.

Like all of the Legerity SLIC devices, the Am79R79 Ringing SLIC device supports on-hook transmission, ring-trip detection, programmable loop-detect threshold, and is available with on-chip polarity reversal. The Am79R79 Ringing SLIC device is a programmable constant-current feed device with two on-chip relay drivers to operate external relays. Several performance grades are available to meet both CCITT and LSSGR requirements, including various longitudinal balance options. This unique device is available in the proven Legerity 75 V bipolar process in the 32-pin PLCC package.

ORDERING INFORMATION

Standard Products

Legerity standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of the elements below



| Valid Combinations | | |
|--------------------|----------------------|----|
| Am79R79 | -1 -2 -3 -4 | JC |

Valid Combinations

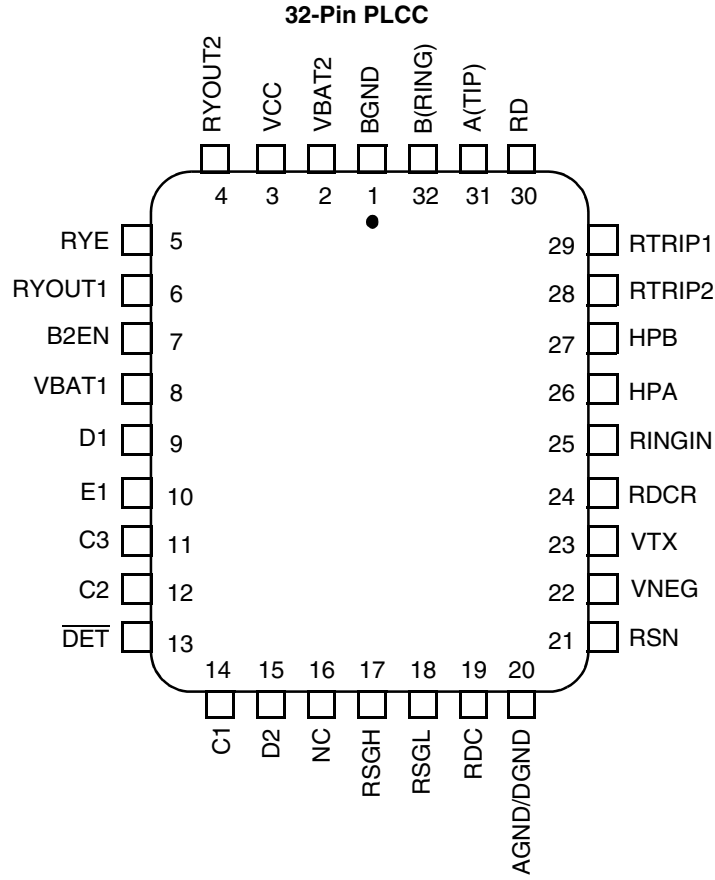
Valid Combinations list configurations planned to be supported in volume for this device. Consult the local Legerity sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on Legerity's standard military-grade products.

Note:

* Functionality of the device from 0°C to +70°C is guaranteed by production testing. Performance from -40°C to +85°C is guaranteed by characterization and periodic sampling of production units.

CONNECTION DIAGRAM

Top View



Notes:

1. Pin 1 is marked for orientation.
2. NC = No connect

PIN DESCRIPTIONS

| Pin Names | Type | Description |
|------------------|-----------|---|
| AGND/DGND | Gnd | Analog and Digital ground |
| A(TIP) | Output | Output of A(TIP) power amplifier |
| B2EN | Input | VBAT2 Enable. Logic Low enables operation from V_{BAT2} . Logic High enables operation from V_{BAT1} . TTL compatible. |
| BGND | Gnd | Battery (power) ground |
| B(RING) | Output | Output of B(RING) power amplifier |
| C3–C1 | Input | Decoder. TTL compatible. C3 is MSB and C1 is LSB. |
| D1 | Input | Relay1 Control. TTL compatible. Logic Low activates the Relay1 relay driver. |
| D2 | Input | (Option) Relay2 Control. TTL compatible. Logic Low activates the Relay2 relay driver. |
| \overline{DET} | Output | Switchhook Detector. Logic Low indicates that the selected detector is tripped. Logic inputs C3–C1 and E1 select the detector. Open-collector with a built-in 15 k Ω pull-up resistor. |
| E1 | Input | (Option) Ground-Key Enable. A logic High selects the off-hook detector. A logic Low selects the ground-key detector. TTL compatible. |
| HPA | Capacitor | High-pass filter capacitor. A(TIP) side of high-pass filter capacitor. |
| HPB | Capacitor | High-pass filter capacitor. B(RING) side of high-pass filter capacitor. |
| RD | Resistor | Detector resistor. Detector threshold set and filter pin. |
| RDC | Resistor | DC feed resistor. Connection point for the DC feed current programming network, which also connects to the receiver summing node (RSN). V_{RDC} is negative for normal polarity and positive for reverse polarity. |
| RDCR | — | Connection point for feedback during ringing. |
| RINGIN | Input | Ring Signal Input. Pin for ring signal input. Square-wave shaped by external RC filter. Requires 50% duty cycle. CMOS-compatible input. |
| RSGH | Input | Saturation Guard High. Pin for resistor to adjust Open Circuit voltage when operating from V_{BAT1} . |
| RSGL | Input | Saturation Guard Low. Pin for resistor to adjust the anti-saturation cut-in voltage when operating from both V_{BAT1} and V_{BAT2} . |
| RSN | Input | Receive Summing Node. The metallic current (AC and DC) between A(TIP) and B(RING) is equal to 1000 x the current into this pin. The networks that program receive gain, two-wire impedance, and feed resistance all connect to this node. |
| RTRIP1 | Input | Ring-trip detector. Ring-trip detector threshold set and filter pin. |
| RTRIP2 | Input | Ring-trip detector. Ring-trip detector threshold offset (switch to V_{BAT1}). For power conservation in any nonringing state, this switch is open. |
| RYE | Output | Common Emitter of RYOUT1/RYOUT2. Emitter output of RYOUT1 and RYOUT2. Normally connected to relay ground. |
| RYOUT1 | Output | Relay/switch driver. Open-collector driver with emitter internally connected to RYE. |
| RYOUT2 | Output | (Option) Relay/switch driver. Open-collector driver emitter internally connected to RYE. |
| VBAT1 | Battery | Battery supply and connection to substrate. |
| VBAT2 | Battery | Power supply to output amplifiers. Connect to off-hook battery through a diode. |
| VCC | Power | Positive analog power supply. |
| VNEG | Power | Negative analog power supply. This pin is the return for the intern VEE regulator. |
| VTX | Output | Transmit Audio. This output is 0.5066 gain version of the A(TIP) and B(RING) metallic voltage. VTX also sources the two-wire input impedance programming network. |

ABSOLUTE MAXIMUM RATINGS

| | |
|--|-----------------------------------|
| Storage temperature | -55°C to +150°C |
| V _{CC} with respect to AGND/DGND | 0.4 V to +7 V |
| V _{NEG} with respect to AGND/DGND | 0.4 V to V _{BAT2} |
| V _{BAT2} | V _{BAT1} to GND |
| V _{BAT1} with respect to AGND/DGND: | |
| Continuous | +0.4 V to -80 V |
| 10 ms | +0.4 V to -85 V |
| BGND with respect to AGND/DGND..... | +3 V to -3 V |
| A(TIP) or B(RING) to BGND: | |
| Continuous | V _{BAT1} -5 V to +1 V |
| 10 ms (f = 0.1 Hz) | V _{BAT1} -10 V to +5 V |
| 1 μs (f = 0.1 Hz) | V _{BAT1} -15 V to +8 V |
| 250 ns (f = 0.1 Hz) | V _{BAT1} -20 V to +12 V |
| Current from A(TIP) or B(RING)..... | ±150 mA |
| RYOUT1, RYOUT2 current..... | 75 mA |
| RYOUT1, RYOUT2 voltage | RYE to +7 V |
| RYOUT1, RYOUT2 transient | RYE to +10 V |
| RYE voltage | BGND to V _{BAT1} |
| C3-C1, D2-D1, E1, B2EN, and RINGIN | |
| Input voltage | -0.4 V to V _{CC} + 0.4 V |
| Maximum power dissipation, continuous, | |
| T _A = 85°C, No heat sink (See note): | |
| In 32-pin PLCC package..... | 1.33 W |
| Thermal data: | θ _{JA} |
| In 32-pin PLCC package..... | 45°C/W typ |

Note: Thermal limiting circuitry on chip will shut down the circuit at a junction temperature of about 165°C. The device should never see this temperature and operation above 145°C junction temperature may degrade device reliability. See the SLIC Packaging Considerations for more information.

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices

| | |
|---------------------------------------|------------------------------|
| Ambient temperature | 0°C to +70°C* |
| V _{CC} | 4.75 V to 5.25 V |
| V _{NEG} | -4.75 V to V _{BAT2} |
| V _{BAT1} | -40.5 V to -75 V |
| V _{BAT2} | -19 V to V _{BAT1} |
| AGND/DGND..... | 0 V |
| BGND with respect to | |
| AGND/DGND | -100 mV to +100 mV |
| Load resistance on VTX to ground..... | 20 kΩ min |

The Operating Ranges define those limits between which the functionality of the device is guaranteed.

* Functionality of the device from 0°C to +70°C is guaranteed by production testing. Performance from -40°C to +85°C is guaranteed by characterization and periodic sampling of production units.

ELECTRICAL CHARACTERISTICS

| Description | Test Conditions (See Note 1) | Min | Typ | Max | Unit | Note | |
|--|---|--------------------|-------|-------|---------------------|---------|------|
| Transmission Performance | | | | | | | |
| 2-wire return loss | 200 Hz to 3.4 kHz (Test Circuit D) | 26 | | | dB | 1, 4, 6 | |
| Z_{VTX} , analog output impedance | | | 3 | 20 | Ω | 4 | |
| V_{VTX} , analog output offset voltage | 0°C to +70°C | -35 | | +35 | mV | 4 | |
| | -40°C to +85°C | -40 | | +40 | | | |
| Z_{RSN} , analog input impedance | | | 1 | 20 | Ω | | |
| Overload level, 2-wire and 4-wire, off hook | Active state | 2.5 | | | Vpk | 2a | |
| Overload level, 2-wire | On hook, $R_{LAC} = 600 \Omega$ | 0.88 | | | Vrms | 2b | |
| THD (Total Harmonic Distortion) | +3 dBm, BAT2 = -24 V | | -64 | -50 | dB | 5 | |
| THD, on hook, OHT state | 0 dBm, $R_{LAC} = 600 \Omega$ BAT1 = -75 V | | | -40 | | | |
| Longitudinal Performance (See Test Circuit C) | | | | | | | |
| Longitudinal to metallic L-T, L-4 balance | 200 Hz to 1 kHz | -1, -3* | 52 | | dB | 4 | |
| | normal polarity | -2, -4 | 63 | | | | |
| | reverse polarity | -2 | 54 | | | | |
| | normal polarity, -40°C to +85°C | -2, -4 | 58 | | | | |
| | 1 kHz to 3.4 kHz | -1, -3* | 52 | | | | |
| | normal polarity | -2, -4 | 58 | | | | |
| | reverse polarity | -2 | 54 | | | | |
| | normal polarity, -40°C to +85°C | -2, -4 | 54 | | | | |
| Longitudinal signal generation 4-L | 200 Hz to 800 Hz normal polarity | 42 | | | | | |
| Longitudinal current per pin (A or B) | Active or OHT state | 12 | 28 | | mArms | 4 | |
| Longitudinal impedance at A or B | 0 to 100 Hz, $T_A = +25^\circ\text{C}$ | | 25 | | Ω/pin | | |
| Idle Channel Noise | | | | | | | |
| C-message weighted noise | 0°C to +70°C | | +7 | +11 | dBrnC | 4 | |
| | -40°C to +85°C | | | +12 | | | |
| Psophometric weighted noise | 0°C to +70°C | | -83 | -79 | dBmp | 4 | |
| | -40°C to +85°C | | | -78 | | | |
| Insertion Loss and Four- to Four-Wire Balance Return Signal (See Test Circuits A and B) | | | | | | | |
| Gain accuracy | 4- to 2-wire | 0 dBm, 1 kHz | -0.20 | 0 | +0.20 | dB | 3 |
| Gain accuracy | 2- to 4-wire and 4- to 4-wire | 0 dBm, 1 kHz | -6.22 | -6.02 | -5.82 | | |
| Gain accuracy | 4- to 2-wire | OHT state, on hook | -0.35 | 0 | +0.35 | | |
| Gain accuracy | 2- to 4-wire and 4- to 4-wire | OHT state, on hook | -6.37 | -6.02 | -5.77 | | |
| Gain accuracy over frequency | 300 to 3400 Hz relative to 1 kHz | 0°C to +70°C | -0.10 | | +0.10 | dB | 3, 4 |
| | | -40°C to +85°C | -0.15 | | +0.15 | | |
| Gain tracking | +3 dBm to -55 dBm relative to 0 dBm | 0°C to +70°C | -0.10 | | +0.10 | dB | 3, 4 |
| | | -40°C to +85°C | -0.15 | | +0.15 | | |
| Gain tracking OHT state, on hook | 0 dBm to -37 dBm +3 dBm to 0 dBm | 0°C to +70°C | -0.10 | | +0.10 | dB | 3 |
| | | -40°C to +85°C | -0.15 | | +0.15 | | |
| Group delay | 0 dBm, 1 kHz | | 3 | | μs | 1, 4, 6 | |

Note:

* Performance Grade

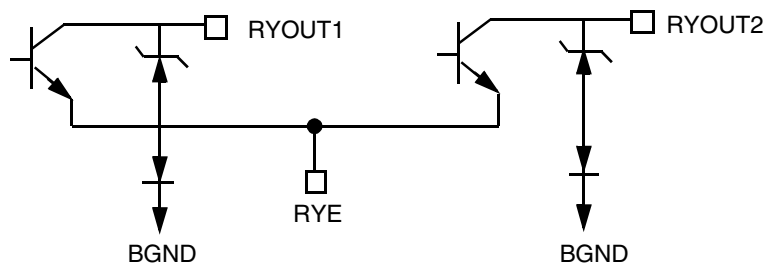
ELECTRICAL CHARACTERISTICS (continued)

| Description | Test Conditions (See Note 1) | Min | Typ | Max | Unit | Note | |
|--|---|---------------------|-------|------------|------|---------------|---|
| Line Characteristics | | | | | | | |
| I_L , Loop-current accuracy | I_L in constant-current region, B2EN = 0 | $0.915I_L$ | I_L | $1.085I_L$ | mA | | |
| I_L , Long loops, Active state | $R_{LDC} = 600 \Omega$, RSGL = open | 20 | 21.7 | | | | |
| | $R_{LDC} = 750 \Omega$, RSGL = short | 20 | | | | | |
| I_L , Accuracy, Standby state | $I_L = \frac{ V_{BAT1} - 10V}{R_L + 400}$ | $0.8I_L$ | I_L | $1.2I_L$ | | | |
| | I_L = constant-current region $T_A = 25^\circ\text{C}$ | 18 | 27 | 39 | | | |
| | -40°C to $+85^\circ\text{C}$ | 18 | 27 | | | | 4 |
| $I_{L\text{LIM}}$ | Active, A and B to ground | | 55 | 110 | | | |
| | OHT, A and B to ground | | 55 | | | | 4 |
| I_L , Loop current, Open Circuit state | $R_L = 0$ | | | 100 | | μA | |
| I_A , Pin A leakage, Tip Open state | $R_L = 0$ | | | 100 | | | |
| I_B , Pin B current, Tip Open state VA, Standby, ground-start signaling | B to ground | | 34 | | mA | | |
| | A to $-48\text{ V} = 7\text{ k}\Omega$, B to ground = $100\ \Omega$ | -7.5 | -5 | | V | 4 | |
| V_{AB} , Open Circuit voltage | | 42.8 | | | | 8 | |
| Power Supply Rejection Ratio ($V_{\text{RIPPLE}} = 100\text{ mVrms}$), Active Normal State | | | | | | | |
| V_{CC} | 50 Hz to 3400 Hz | 33 | 50 | | dB | 5 | |
| V_{NEG} | 50 Hz to 3400 Hz | 30 | 40 | | | | |
| V_{BAT1} | 50 Hz to 3400 Hz | 30 | 50 | | | | |
| V_{BAT2} | 50 Hz to 3400 Hz | 30 | 50 | | | | |
| Power Dissipation | | | | | | | |
| On hook, Open Circuit state | V_{BAT1} | | 48 | 100 | mW | | |
| On hook, Standby state | V_{BAT2} | | 55 | 80 | | 10 | |
| On hook, OHT state | V_{BAT1} | | 200 | 300 | | | |
| On hook, Active state | V_{BAT1} | | 220 | 350 | | | |
| Off hook, Standby state | V_{BAT1} or V_{BAT2} | $R_L = 300\ \Omega$ | 2000 | 2800 | | 10 | |
| Off hook, OHT state | V_{BAT1} | $R_L = 300\ \Omega$ | 2000 | 2200 | | | |
| Off hook, Active state | V_{BAT2} | $R_L = 300\ \Omega$ | 550 | 750 | | | |
| Supply Currents | | | | | | | |
| I_{CC} , On-hook V_{CC} supply current | Open Circuit state | | 3.0 | 4.5 | mA | | |
| | Standby state | | 3.2 | 5.5 | | | |
| | OHT state | | 6.2 | 8.0 | | | |
| | Active state–normal | | 6.5 | 9.0 | | | |
| I_{NEG} , On-hook V_{NEG} supply current | Open Circuit state | | 0.1 | 0.2 | | | |
| | Standby state | | 0.1 | 0.2 | | | |
| | OHT state | | 0.7 | 1.1 | | | |
| | Active state–normal | | 0.7 | 1.1 | | | |
| I_{BAT} , On-hook V_{BAT} supply current | Open Circuit state | | 0.45 | 1.0 | | | |
| | Standby state | | 0.6 | 1.5 | | | |
| | OHT state | | 2.0 | 4.0 | | | |
| | Active state–normal | | 2.7 | 5.0 | | | |

ELECTRICAL CHARACTERISTICS (continued)

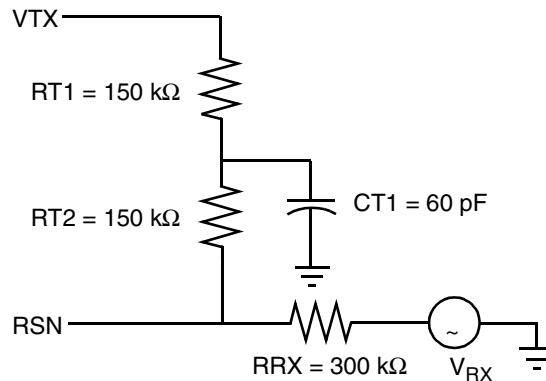
| Description | Test Conditions (See Note 1) | Min | Typ | Max | Unit | Note |
|--|--|------|-------|------|-----------------|------|
| Logic Inputs (C3–C1, D2–D1, E1, and B2EN) | | | | | | |
| V _{IH} , Input High voltage | | 2.0 | | | V | |
| V _{IL} , Input Low voltage | | | | 0.8 | | |
| I _{IH} , Input High current | | –75 | | 40 | μA | |
| I _{IL} , Input Low current | | –400 | | | | |
| Logic Output DET | | | | | | |
| V _{OL} , Output Low voltage | I _{OUT} = 0.8 mA, 15 kΩ to V _{CC} | | | 0.40 | V | |
| V _{OH} , Output High voltage | I _{OUT} = –0.1 mA, 15 kΩ to V _{CC} | 2.4 | | | | |
| Ring-Trip Detector Input | | | | | | |
| Ring detect accuracy | $IRTD = \left(\frac{ BAT1 - 1}{RRT1} + 24 \mu A \right) \cdot 335$ | –10 | | +10 | % | |
| Ring Signal | | | | | | |
| V _{AB} , Ringing | Bat1 = –75 V, ringload = 1570 Ω | 66 | 69 | | V _{pk} | 7 |
| V _{AB} Ringing offset | V _{RINGIN} = 2.5 V | –10 | 0 | 10 | V | |
| ΔV _{AB} /ΔV _{RINGIN} (RINGIN gain) | | 150 | 180 | 210 | | |
| Ground-Key Detector Thresholds | | | | | | |
| Ground-key resistive threshold | B to ground | 2 | 5 | 10 | kΩ | |
| Ground-key current threshold | B to ground | | 11 | | mA | |
| Loop Detector | | | | | | |
| R _{LTH} , Loop-resistance detect threshold | Active, V _{BAT1} | –20 | | 20 | % | 9 |
| | Active, V _{BAT2} | –20 | | 20 | | |
| | Standby | –12 | | 12 | | |
| Relay Driver Output (RELAY1 and 2) | | | | | | |
| V _{OL} , On voltage (each output) | I _{OL} = 30 mA | | +0.25 | +0.4 | V | 4 |
| V _{OL} , On voltage (each output) | I _{OL} = 40 mA | | +0.30 | +0.8 | | |
| I _{OH} , Off leakage (each output) | V _{OH} = +5 V | | | 100 | μA | |
| Zener breakover (each output) | I _Z = 100 μA | 6.6 | 7.9 | | V | |
| Zener on voltage (each output) | I _Z = 30 mA | | 11 | | | |

RELAY DRIVER SCHEMATIC



Notes:

- Unless otherwise noted, test conditions are $BAT1 = -75\text{ V}$, $BAT2 = -24\text{ V}$, $V_{CC} = +5\text{ V}$, $V_{NEG} = -5\text{ V}$, $R_L = 600\ \Omega$, $R_{DC1} = 80\text{ k}\Omega$, $R_{DC2} = 20\text{ k}\Omega$, $R_D = 75\text{ k}\Omega$, no fuse resistors, $C_{HP} = 0.018\ \mu\text{F}$, $C_{DC} = 1.2\ \mu\text{F}$, $D_1 = D_2 = 1\text{N}400\text{x}$, two-wire AC input impedance (ZSL) is a $600\ \Omega$ resistance synthesized by the programming network shown below. $R_{SGL} = \text{open}$, $R_{SGH} = \text{open}$, $R_{DCR} = 2\text{ k}\Omega$, $R_{RT1} = 430\text{ k}\Omega$, $R_{RT2} = 12\text{ k}\Omega$, $C_{RT} = 1.5\ \mu\text{F}$, $R_{SLEW} = 100\text{ k}\Omega$, $C_{SLEW} = 0.33\ \mu\text{F}$.



- Overload level is defined when $THD = 1\%$.
 - Overload level is defined when $THD = 1.5\%$.
- Balance return signal is the signal generated at V_{TX} by V_{RX} . This specification assumes that the two-wire AC load impedance matches the programmed impedance.
- Not tested in production. This parameter is guaranteed by characterization or correlation to other tests.
- This parameter is tested at 1 kHz in production. Performance at other frequencies is guaranteed by characterization.
- Group delay can be greatly reduced by using a Z_T network such as that shown in Note 1 above. The network reduces the group delay to less than $2\ \mu\text{s}$ and increases 2WRL . The effect of group delay on linecard performance may also be compensated for by synthesizing complex impedance with the QSLAC or DSLAC device.
- 70 Vpk provides 50 Vrms with a crest factor of 1.25 to a load of $1400\ \Omega$ with $2 \cdot R_f = 100$, and $R_{line} = 70\ \Omega$ ($1570\ \Omega$).
- Open Circuit V_{AB} can be modified using R_{SGH} .
- R_D must be greater than $56\text{ k}\Omega$. Refer to Table 2 for typical value of R_{LTH} .
- Lower power is achieved by switching into low-battery state in standby. Standby loop current is returned to V_{BAT1} regardless of the battery selected.

Table 1. SLIC Decoding

| State | C3 C2 C1 | 2-Wire Status | (DET) Output | | Battery Selection |
|-------|----------|--------------------------|---------------|------------|-------------------|
| | | | E1 = 1 | E1 = 0 | |
| 0 | 0 0 0 | Open Circuit | Ring trip | Ring trip | B2EN |
| 1 | 0 0 1 | Ringing | Ring trip | Ring trip | |
| 2 | 0 1 0 | Active | Loop detector | Ground key | |
| 3 | 0 1 1 | On-hook TX (OHT) | Loop detector | Ground key | |
| 4 | 1 0 0 | Tip Open | Loop detector | Ground key | B2EN = 1** |
| 5 | 1 0 1 | Standby | Loop detector | Ground key | V_{BAT1} |
| 6* | 1 1 0 | Active Polarity Reversal | Loop detector | Ground key | B2EN |
| 7* | 1 1 1 | OHT Polarity Reversal | Loop detector | Ground key | |

Notes:

* Only -1 and -2 performance grade devices support polarity reversal.

** For correct ground-start operation using Tip Open, V_{BAT1} on-hook battery must be used.

Table 2. User-Programmable Components

| | |
|--|---|
| $Z_T = 500(Z_{2WIN} - 2R_F)$ | <p>Z_T is connected between the VTX and RSN pins. The fuse resistors are R_F, and Z_{2WIN} is the desired 2-wire AC input impedance. When computing Z_T, the internal current amplifier pole and any external stray capacitance between VTX and RSN must be taken into account.</p> |
| $Z_{RX} = \frac{Z_L}{G_{42L}} \cdot \frac{1000 \cdot Z_T}{Z_T + 500(Z_L + 2R_F)}$ | <p>Z_{RX} is connected from V_{RX} to R_{SN}. Z_T is defined above, and G_{42L} is the desired receive gain.</p> |
| $R_{DC1} + R_{DC2} = \frac{2500}{I_{LOOP}}$ $R_{DCR1} + R_{DCR2} = \frac{3000}{I_{ringlim}}$ $C_{DC} = 19 \text{ ms} \cdot \frac{R_{DC1} + R_{DC2}}{R_{DC1}R_{DC2}}$ $C_{DCR} = \frac{R_{DCR1} + R_{DCR2}}{R_{DCR1}R_{DCR2}} \cdot 150 \text{ } \mu\text{s}$ | <p>R_{DC1}, R_{DC2}, and C_{DC} form the network connected to the RDC pin. I_{LOOP} is the desired loop current in the constant-current region.</p> <p>R_{DCR1}, R_{DCR2}, and C_{DCR} form the network connected to the RDCR pin. See Applications Circuit for these components.</p> <p>C_{DCR} sets the ringing time constant, which can be between 15 μs and 150 μs.</p> |
| $R_D = R_{LTH} \cdot 12.67 \text{ for high battery state}$ | <p>R_D is the resistor connected from the RD pin to GND and R_{LTH} is the loop-resistance threshold between on-hook and off-hook detection. R_D should be greater than 56 kΩ to guarantee detection occurs in the Standby state. Choose the value of R_D for high battery state; then use the equation for R_{LTH} to find where the threshold is for low battery.</p> |
| Loop-Threshold Detect Equations | |
| $R_{LTH} = \frac{R_D}{12.67} \text{ for high battery}$ | <p>This is the same equation as for R_D above, except solved for R_{LTH}.</p> |
| $R_{LTH} = \frac{R_D}{11.37} \text{ for low battery}$ | <p>For low battery, the detect threshold is slightly higher, which avoids oscillating between states.</p> |
| $R_{LTH} = \frac{ V_{BAT1} - 10}{915} \cdot R_D - 400 - 2R_F$ | <p>$R_{LTH \text{ standby}} < R_{LTH \text{ active}} < V_{BAT1} < R_{LTH \text{ active}} < V_{BAT2}$, which guarantees no unstable states under all operating conditions. This equation shows at what resistance the standby threshold is; it is actually a current threshold rather than a resistance threshold, which is shown by the Vbat dependency.</p> |

DC FEED CHARACTERISTICS

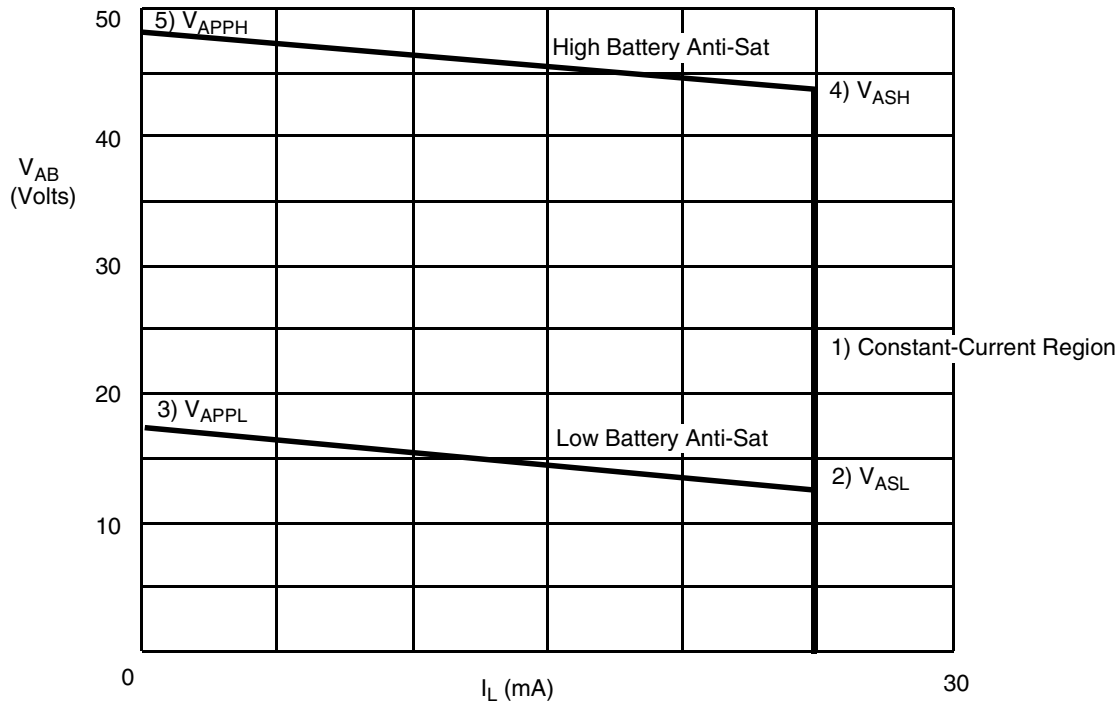


Figure 1. Typical V_{AB} vs. I_L DC Feed Characteristics

$$R_{DC} = R_{DC1} + R_{DC2} = 20 \text{ k}\Omega + 80 \text{ k}\Omega = 100 \text{ k}\Omega$$

$$(V_{BAT1} = -75 \text{ V}, V_{BAT2} = -24 \text{ V})$$

Notes:

1. Constant-current region: $V_{AB} = I_L R_L = \frac{2500}{RDC} R_L$; where $R_L = R_L + 2R_F$,

2. Low battery $V_{ASL} = \frac{1000 \cdot (104 \cdot 10^3 + R_{SGL})}{6720 \cdot 10^3 + (80 \cdot R_{SGL})}$; where R_{SGL} = resistor to GND, B2EN = logic Low.

Anti-sat region: $V_{ASL} = \frac{1000 \cdot (R_{SGL} - 56 \cdot 10^3)}{6720 \cdot 10^3 + (80 \cdot R_{SGL})}$; where R_{SGL} = resistor to V_{CC} , B2EN = logic Low.
 R_{SGL} to V_{CC} must be greater than 100 k Ω .

3. $V_{APPL} = 4.17 + V_{ASL}$
 $I_{LOOP} = \frac{V_{APPL}}{\frac{(R_{DC1} + R_{DC2})}{600} + 2R_F + R_{LOOP}}$

4. High battery $V_{ASH} = V_{ASHH} + V_{ASL}$
 Anti-sat region: $V_{ASHH} = \frac{1000 \cdot (70 \cdot 10^3 + R_{SGH})}{1934 \cdot 10^3 + (31.75 \cdot R_{SGH})}$; where R_{SGH} = resistor to GND, B2EN = logic High.

$V_{ASHH} = \frac{1000 \cdot (R_{SGH} + 2.75 \cdot 10^3)}{1934 \cdot 10^3 + (31.75 \cdot R_{SGH})}$; where R_{SGH} = resistor to V_{CC} , B2EN = logic High.
 R_{SGH} to V_{CC} must be greater than 100 k Ω .

5. $V_{APPH} = 4.17 + V_{ASH}$
 $I_{LOOPH} = \frac{V_{APPH}}{\frac{(R_{DC1} + R_{DC2})}{600} + 2R_F + R_{LOOP}}$

RING-TRIP COMPONENTS

$$R_{RT2} = 12 \text{ k}\Omega$$

$$C_{RT} = 1.5 \text{ }\mu\text{F}$$

$$R_{RT1} = 320 \cdot CF \cdot \frac{V_{BAT1}}{V_{BAT1} - 5 - (24 \text{ }\mu\text{A} \cdot 320 \cdot CF \cdot (R_{LRT} + 150 + 2R_F))} \cdot (R_{LRT} + 150 + 2R_F)$$

where R_{LRT} = Loop-detection threshold resistance for ring trip and CF = Crest factor of ringing signal (≈ 1.25)

R_{SLEW} , C_{SLEW}

Ring waveform rise time $\approx 0.214 \cdot (R_{SLEW} \cdot C_{SLEW}) \approx tr$.

For a 1.25 crest factor @ 20 Hz, $tr \approx 10 \text{ mS}$.

$\therefore (R_{SLEW} = 150 \text{ k}\Omega, C_{SLEW} = 0.33 \text{ }\mu\text{F})$

C_{SLEW} should be changed if a different crest factor is desired.

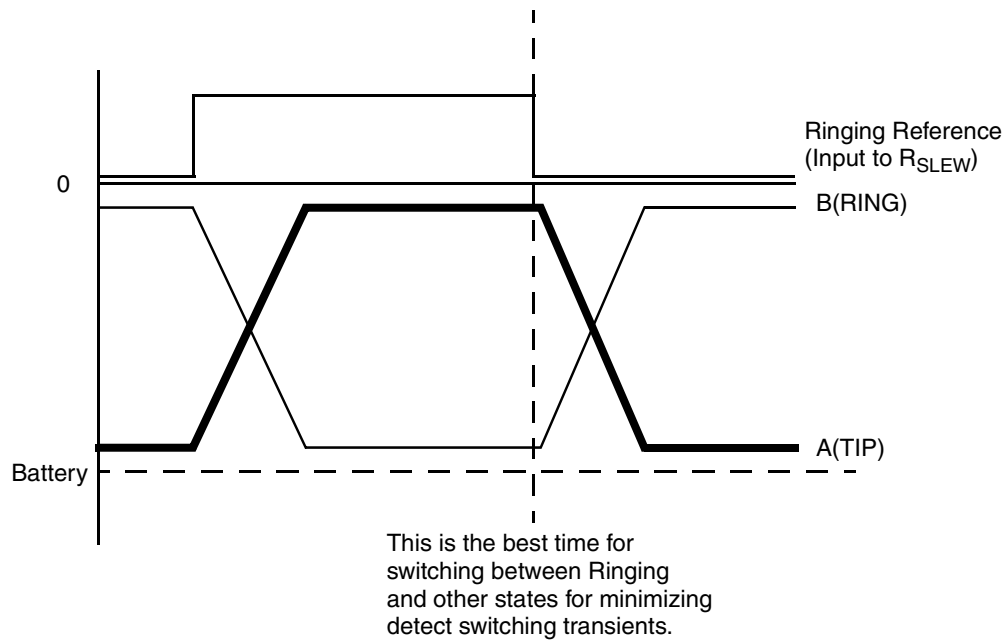
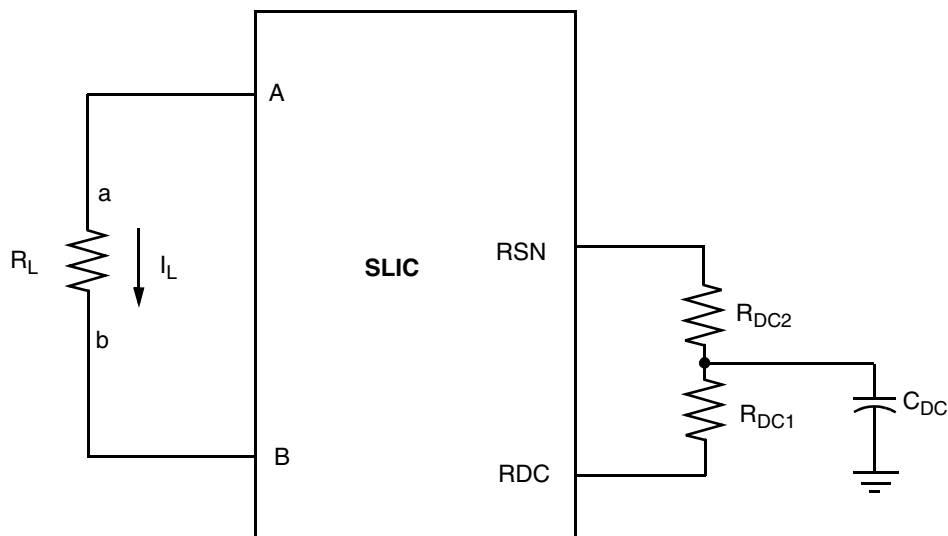


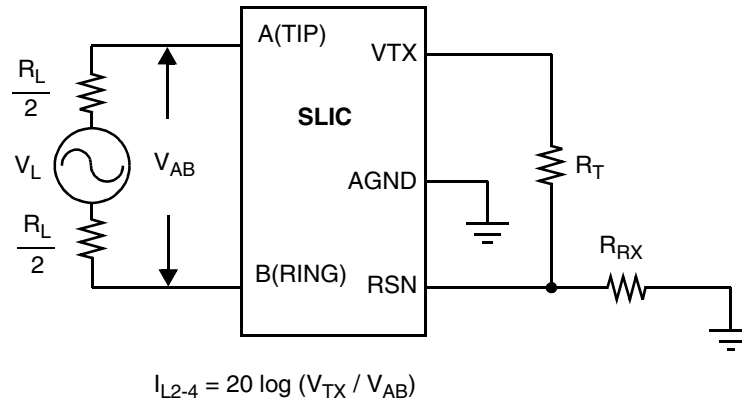
Figure 2. Ringing Waveforms



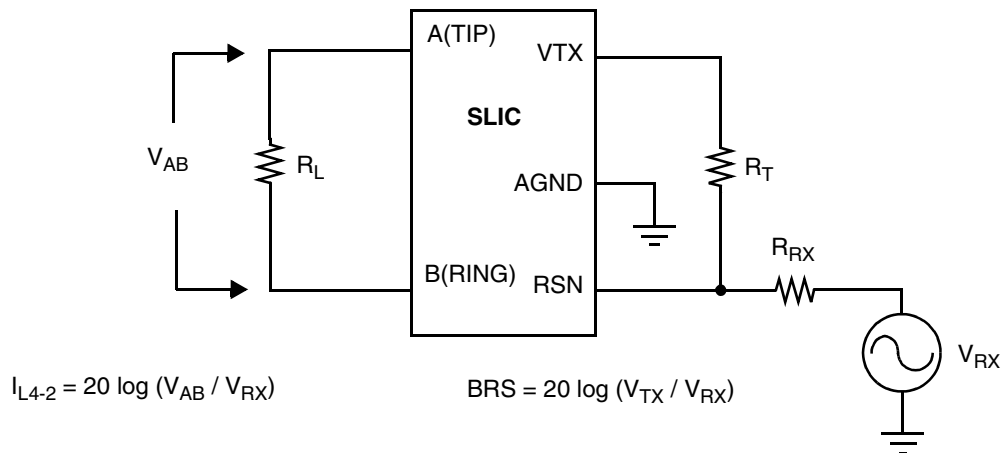
Feed current programmed by R_{DC1} and R_{DC2}

Figure 3. Feed Programming

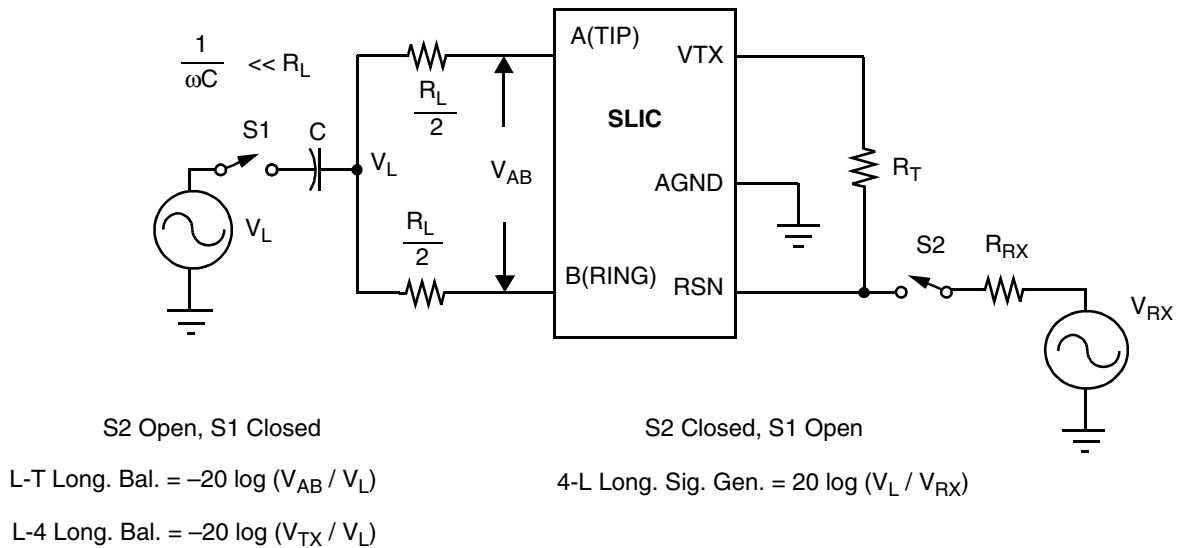
TEST CIRCUITS



A. Two- to Four-Wire Insertion Loss

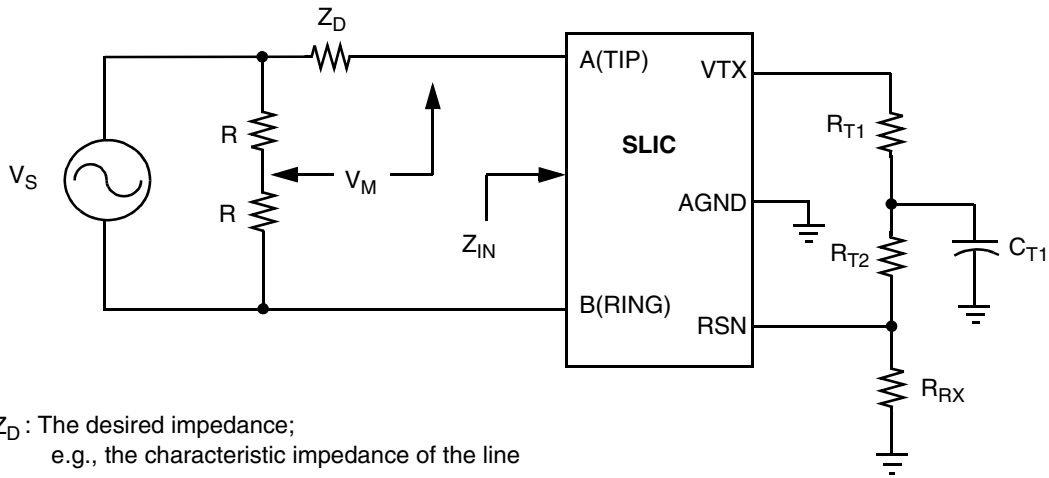


B. Four- to Two-Wire Insertion Loss and Four- to Four-Wire Balance Return Signal



C. Longitudinal Balance

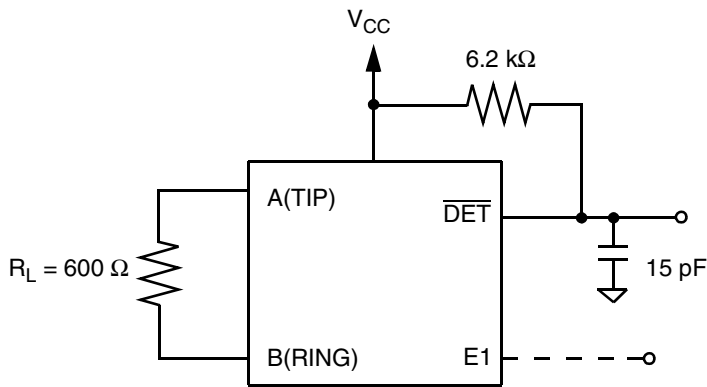
TEST CIRCUITS (continued)



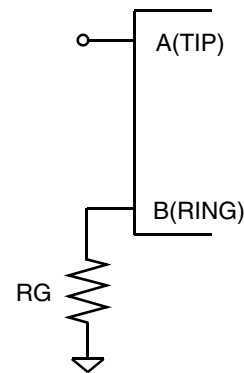
Z_D : The desired impedance;
e.g., the characteristic impedance of the line

$$\text{Return loss} = -20 \log (2 V_M / V_S)$$

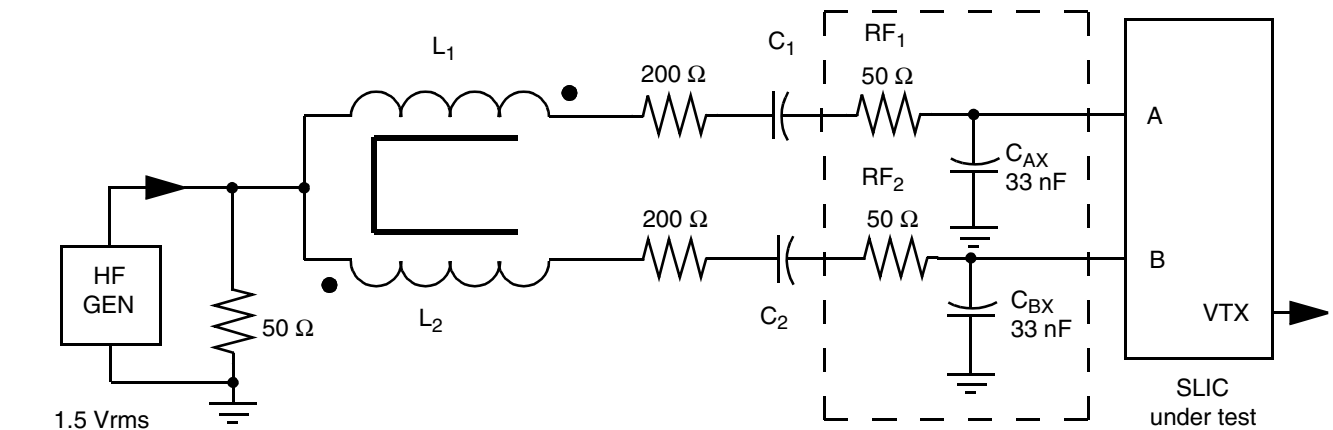
D. Two-Wire Return Loss Test Circuit



E. Loop-Detector Switching

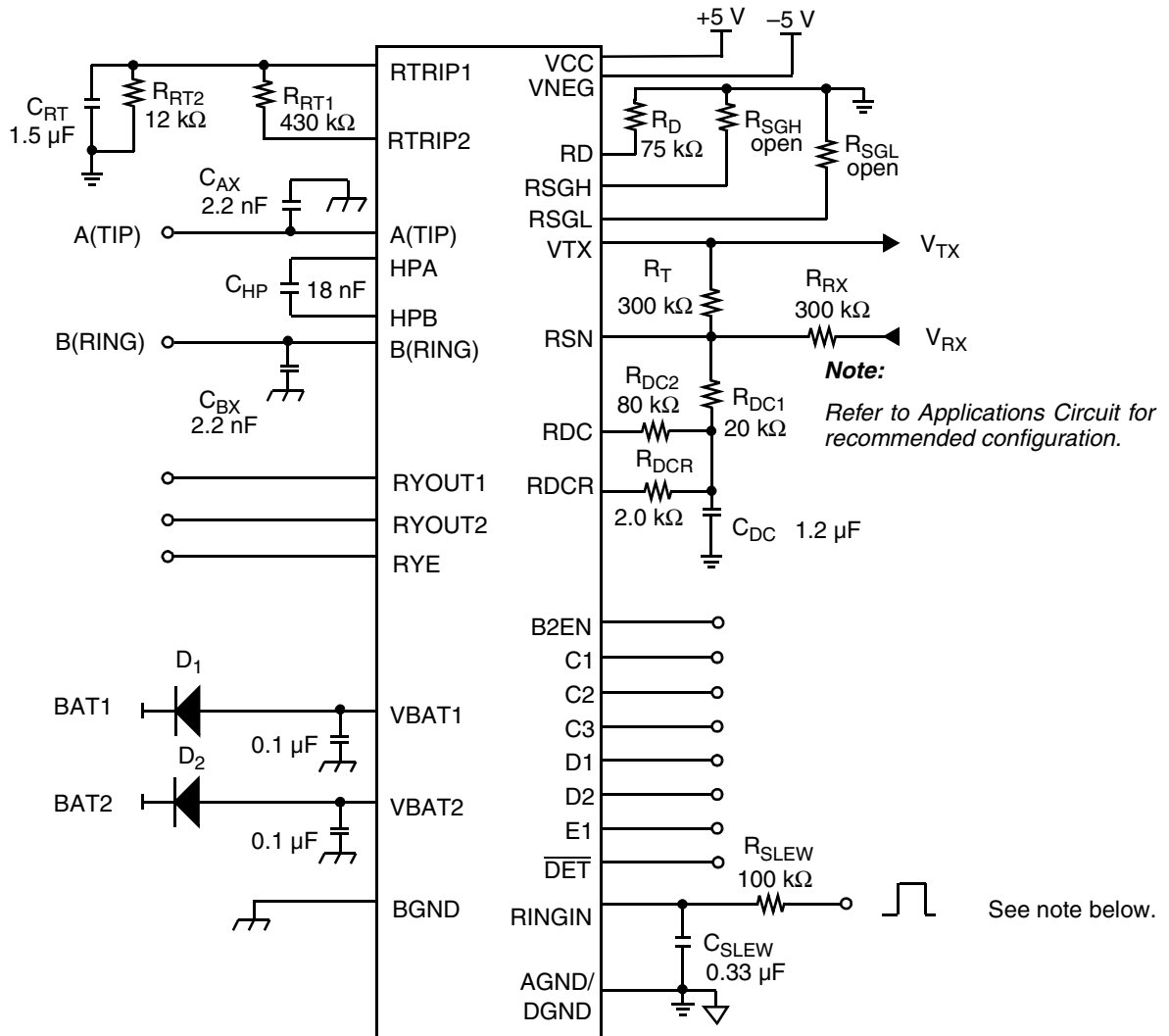


F. Ground-Key Switching



G. RFI Test Circuit

TEST CIRCUITS (continued)



Note:

The input should be 50% duty cycle CMOS-compatible input.

BATTERY GROUND



ANALOG GROUND

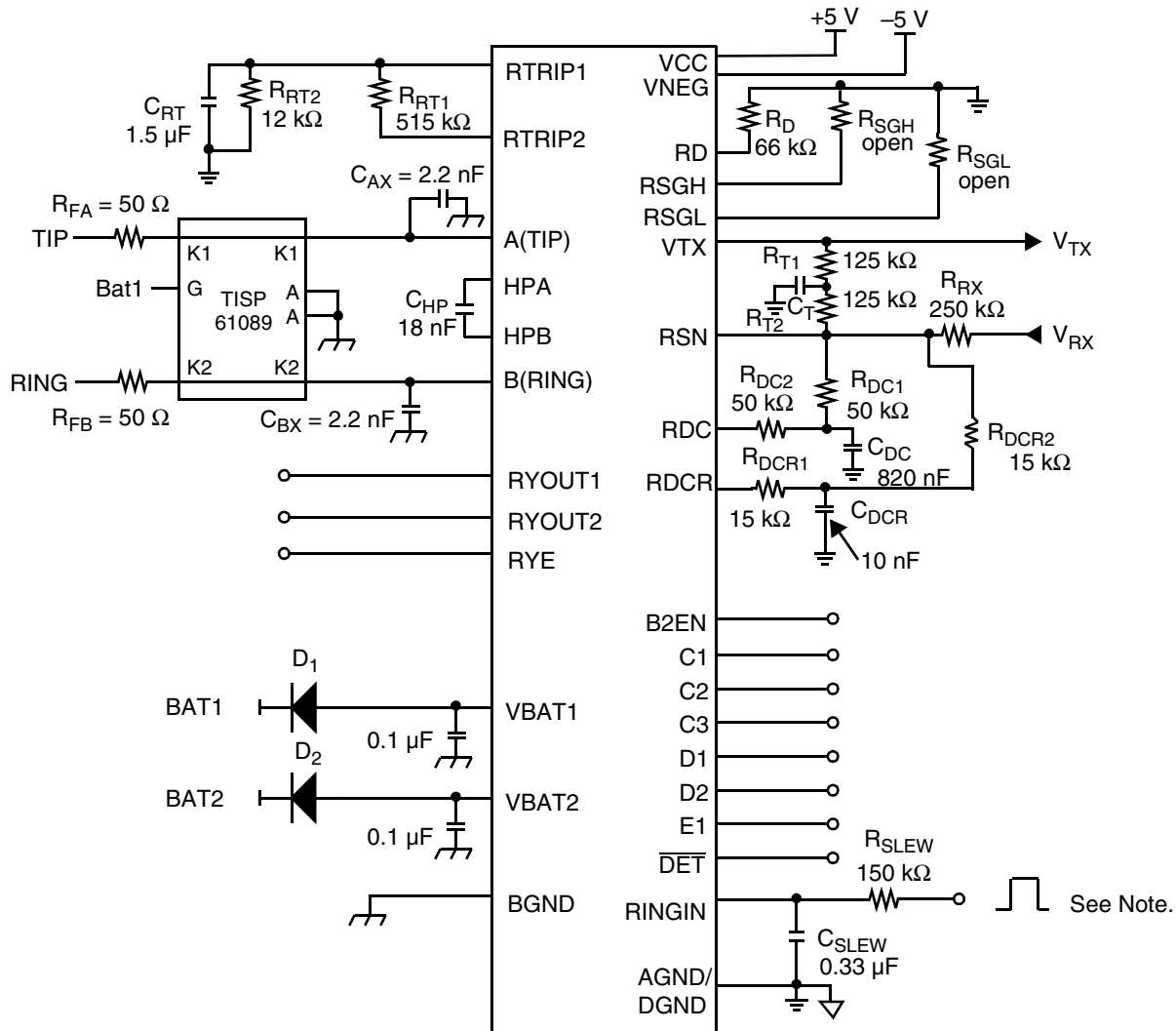


DIGITAL GROUND



H. Am79R79 Test Circuit

APPLICATION CIRCUIT



Assumptions:

- | | | |
|---------------------------------|--|-----------------------------|
| 1. 1.25 CF | 4. 5.2 kΩ High Battery Loop Threshold | 7. $G_{42L} = 1$ |
| 2. 25 mA I_{LOOP} | 5. 925 Ω Ringing Loop Threshold | 8. -70 V Vbat1, -24 V Vbat2 |
| 3. 100 mA Ringing Current Limit | 6. 600 Ω Two-wire Impedance, 600 Ω Z_L | |

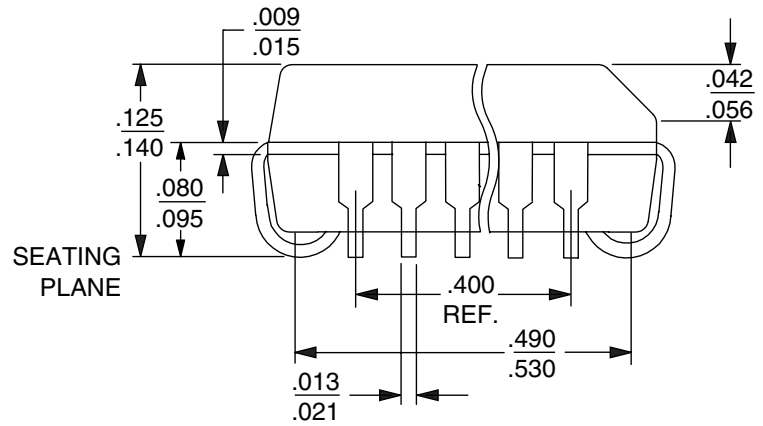
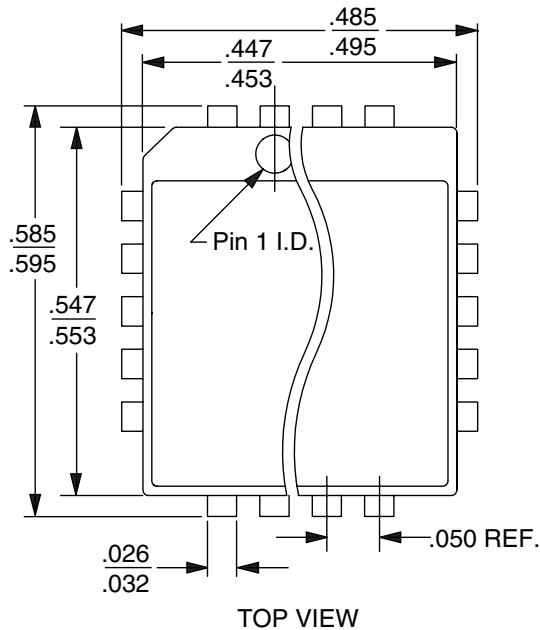
Note:

The input should be 50% duty cycle CMOS-compatible input.

I. Application Circuit

PHYSICAL DIMENSIONS

PL032



16-038FPO-5
PL 032
DA79
6-28-94 ae

REVISION SUMMARY

Revision B to Revision C

- Minor changes were made to the data sheet style and format to conform to Legerity standards.
- Electrical Characteristics; Last row under Ring Signal, min changed from 130 to 150, typ changed from 160 to 180, and max changed from 190 to 210.
- SLIC Decoding Table; Added B2EN reference to the Battery Selection column and its corresponding note to the notes section.
- Applications Circuit; Revised

Revision C to Revision D

- Minor changes were made to the data sheet style and format to conform to Legerity standards.

Revision D to Revision E

- On pages 17 and 18, R_{DC1} and R_{DC2} were switched.

Revision E to Revision F

- The physical dimensions (PL032) were added to the Physical Dimensions section.
- Deleted the Ceramic DIP and Plastic DIP packages and references to them.
- Updated the Pin Description table to correct inconsistencies.

Revision F to Revision G

- The equation on page 13 was changed:

from:
$$R_{RT1} = 300 \cdot CF \cdot \frac{V_{BAT1}}{V_{bat} - 3.5 - (15 \mu A \cdot 300 \cdot CF \cdot (R_{LRT} + 150 + 2R_F))} \cdot (R_{LRT} + 150 + 2R_F)$$

to:
$$R_{RT1} = 320 \cdot CF \cdot \frac{V_{BAT1}}{V_{bat} - 5 - (24 \mu A \cdot 320 \cdot CF \cdot (R_{LRT} + 150 + 2R_F))} \cdot (R_{LRT} + 150 + 2R_F)$$

The contents of this document are provided in connection with Legerity, Inc. products. Legerity makes no representations or warranties with respect to the accuracy or completeness of the contents of this publication and reserves the right to make changes to specifications and product descriptions at any time without notice. No license, whether express, implied, arising by estoppel or otherwise, to any intellectual property rights is granted by this publication. Except as set forth in Legerity's Standard Terms and Conditions of Sale, Legerity assumes no liability whatsoever, and disclaims any express or implied warranty, relating to its products including, but not limited to, the implied warranty of merchantability, fitness for a particular purpose, or infringement of any intellectual property right.

Legerity's products are not designed, intended, authorized or warranted for use as components in systems intended for surgical implant into the body, or in other applications intended to support or sustain life, or in any other application in which the failure of Legerity's product could create a situation where personal injury, death, or severe property or environmental damage may occur. Legerity reserves the right to discontinue or make changes to its products at any time without notice.

© 1999 Legerity, Inc.

All rights reserved.

Trademarks

Legerity, the Legerity logo, and combinations thereof, DSLAC and QSLAC are trademarks of Legerity, Inc.

Other product names used in this publication are for identification purposes only and may be trademarks of their respective companies.



P.O. Box 18200
Austin, Texas 78760-8200

Telephone: (512) 228-5400
Fax: (512) 228-5510
North America Toll Free: (800) 432-4009

*To contact the Legerity Sales Office nearest you,
or to download or order product literature, visit
our website at **www.legerity.com**.*

*To order literature in North America, call:
(800) 572-4859
or email:
americalit@legerity.com*

*To order literature in Europe or Asia, call:
44-0-1179-341607
or email:
Europe — eurolit@legerity.com
Asia — asialit@legerity.com*